IMPLEMENTATION OF RF/MICROWAVE RECEIVER COMPONENTS ON A SEMI-CUSTOM SILICON BIPOLAR ARRAY

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Abstract

The analog transistor array *starCHIP*™ 1 has been developed for rapid, cost-effective design and delivery of many RF/microwave components for applications to 5 GHz. The array is based on silicon bipolar devices with 10 GHz f_T and 20 GHz f_{max} and thin-film polysilicon resistors with low parasitic capacitance and excellent matching. This paper presents an overview of the array topology and technology. The implementation of receiver functions and their measured results is also illustrated with a frequency doubler, a vector demodulator, a limiting amplifier and a phase detector with on-chip VCO. All these components are wideband, require no external baluns, have 50 Ω input and output impedance matching, and operate from a single 5 V power supply.

Introduction

Recent advances in silicon bipolar IC technologies have produced monolithic microwave products for applications well above 1 GHz [1,2,3]. In general, silicon MMIC's can offer higher reliability, reduced size, reduced power consumption and lower cost (in sufficient volumes) when compared to traditional hybrid circuit approaches. However, MMIC's also potentially require larger non-recurring engineering (NRE) costs, longer development times and less flexibility for minor functional changes than equivalent hybrid solutions.

Semi-custom silicon MMIC arrays offer a compromise solution which can combine many of the advantages of both full-custom IC's and hybrid circuits [4,5]. Analog transistor arrays provide a preset grid of transistors and resistors which a MMIC designer can utilize to perform a desired function by specifying one or two layers of metal interconnects. With semi-custom arrays the development time from concept to prototype die is only a few weeks. Minor changes or different versions can be implemented with very little additional NRE charges and project delay. Furthermore, for small to moderate production volumes (typically < 10,000 units/year), the semi-custom array is more cost-effective than full-custom foundry service due to both the lower initial NRE cost and the efficiency of having about 90% of the semiconductor fabrication work common for all products on a given array.

This paper describes the process technology and layout topology of Avantek's first application-specific integrated circuit (ASIC), the *starCHIP*™ 1 . The paper also summarizes the development procedure and test results for several receiver components that have already been implemented on the *starCHIP*™ 1 .

Process Overview

Figure 1 gives an overall cross-section of transistors, resistors and interconnects available with the *ISOSAT*™ II technology. The bipolar devices feature .6 μm nitride self-aligned emitters on a 2 μm emitter-base pitch. The fully ion-implanted structure has shallow emitters and active basewidths below 100 nm. These devices have a peak f_T of 10 GHz and peak f_{max} of 20 GHz for a standard collector profile that allows typical $BV_{CEO} > 12$ V and $BV_{CBO} > 20$ V. Other available collector profiles for digital applications feature f_T to 20 GHz with $BV_{CEO} \sim 4$ V. Resistors are formed by thin-film polysilicon deposition on field oxide for minimal parasitic capacitance and excellent local matching.

Parasitics are minimized throughout the *ISOSAT*™ II process. A global buried layer and deep collector plug keeps collector resistance low. In addition, the global buried layer provides a good RF ground plane at a depth of only a few μm from the metal interconnections on the die. Polyimide-filled trench isolation minimizes collector-substrate capacitance and a 2 μm thick field oxide greatly reduces the parasitic capacitance of first metal and thin-film polysilicon resistors. The thick field oxide isolates the parasitic collector-base sidewall junction and increases the device breakdown voltages. *ISOSAT*™ II features a "true" second metal capability (as opposed to air bridges) for layout ease while maintaining low parasitic capacitance due to its thick polyimide dielectric spacer. Wafers are backlapped to a thickness of only 6 mil. to reduce the thermal resistance of *ISOSAT*™ II products and to ease assembly in small packages.

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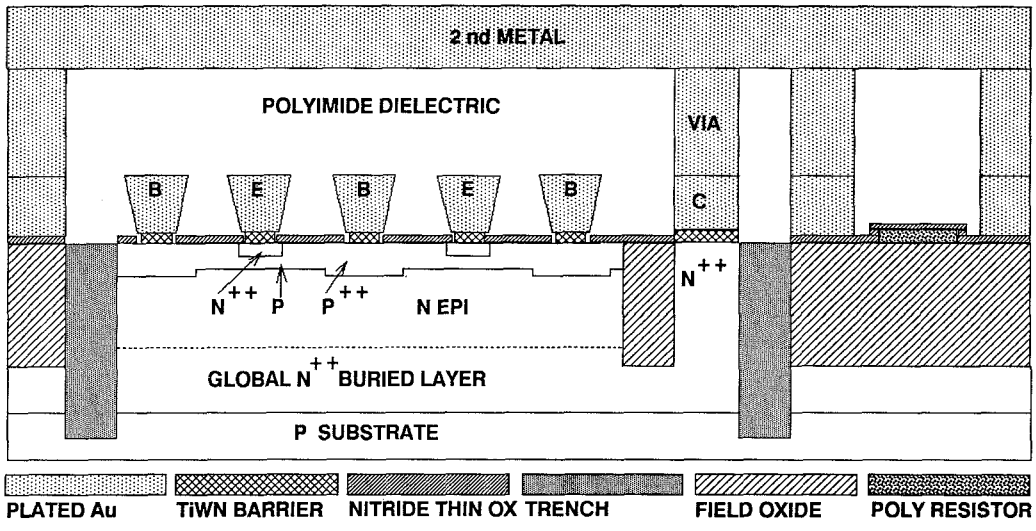

Figure 1. Cross-section of the *ISOSAT*™ II process

starCHIP™ 1 Array Topology

The *starCHIP*™ 1 silicon array contains 92 high-speed, low-noise *npn* transistors and 394 low-parasitic, thin-film resistors. Some thin-film capacitance can also be realized on-chip.

As shown in Figure 2, the 40×60 mil. *starCHIP*™ 1 die is organized into 4 symmetric tile arrays separated by tightly-packed resistor/capacitor arrays and surrounded by 24 bond pads and 20 extra transistors. Each tile array contains 18 *npn* transistors and 3 variable resistor arrays. Resistors are easily combined in series and/or parallel to produce desired values. Typical resistor data is given in Table 1. Practical resistor values vary from 5 Ω to 10 kΩ. Four different transistor sizes are available as summarized in Table 2. The transistors are arranged for easy layout as differential pairs, Gilbert cells, or Darlingtons. Some typical DC device characteristics are given in Table 3 for the most common transistor on *starCHIP*™ 1 (the 40420). Thin-film, on-chip capacitance is available by using metal 1 and the 1000 Ω polysilicon resistors separated by Si_3N_4 and SiO_2. Practical values of capacitance are .2–5 pF with a dielectric strength of at least 40 V.

Adequate component spacing and a full two-level metal capability (2 μm line/space in metal 1) permits easy routing and high component utilization. Both metal layers are approximately 1 μm thick plated gold. Components built on this process have been shown through accelerated life testing to exhibit a predicted median time to failure (MTTF) exceeding 10^7 hrs at 150 °C junction temperature when designed using the *starCHIP*™ 1 metal design rules. The individual devices within the tile arrays are separated enough that virtually all the transistors can be utilized in most designs. The tiles are separated typically 50 μm from the pads and center resistor arrays so that large power busses can be constructed to supply current without exceeding the electromigration limits of the gold metallization.

The 24 low-parasitic 2 mil bond pads allow for flexible pin-outs, multiple in-package capacitors, and easy probing of critical internal circuit nodes. A photograph of the blank *starCHIP*™ 1 array as fabricated up to metal layer 1 is shown in Figure 3.

Because the device sizes on an analog transistor array are fixed, optimizing a design for maximum RF performance consists mainly of selecting resistor values. In this respect, the *starCHIP*™ 1 is superior to existing lower frequency analog arrays since the variable resistor arrays within the *starCHIP*™ 1 tiles offer considerable flexibility. In general, power consumption for a given RF function can be reduced somewhat at the expense of bandwidth. The *starCHIP*™ 1 has basically been optimized for applications where the component output powers will be 0–5 dBm into 50 Ω. For most circuits which utilize a large percentage of the array, the supply current typically totals 50–100 mA if designed for peak RF performance. In cases where overall temperature rise and/or temperature variations on the die cause concern, a computed-aided engineering tool (THEATRIC) is available to provide detailed thermal analyses [6]. For applications which require very low supply currents, *starCHIP*™ 1 designs can be scaled down on full-custom layouts or transferred to future *starCHIP*™ products optimized for low power operation.

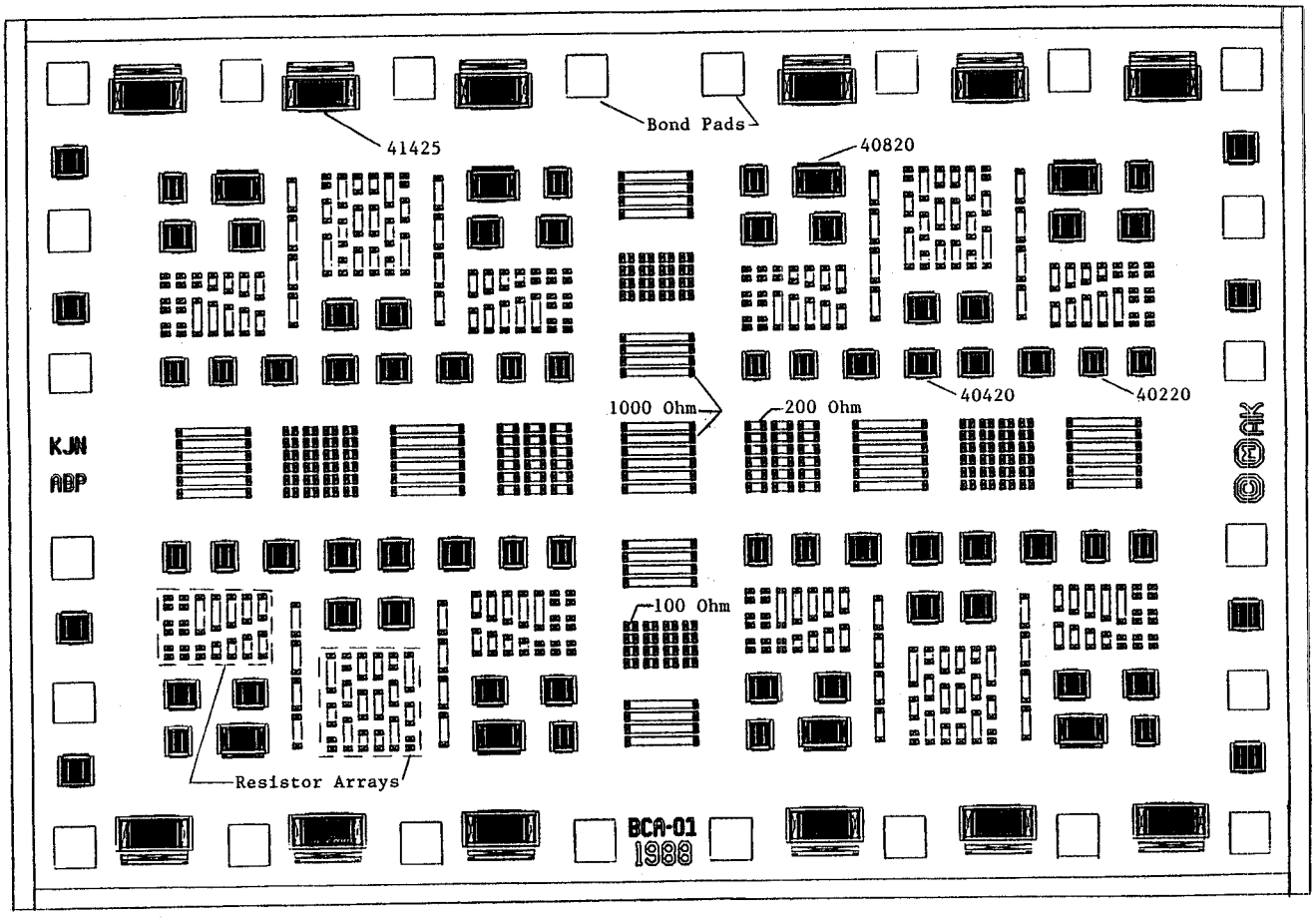

Figure 2. Layout of the *starCHIP*™ 1 array

Example Component Implementations

Wideband Frequency Doubler

Several RF/microwave components have already been successfully implemented on the *starCHIP*™ 1 . One example is a wideband frequency doubler shown conceptually in Figure 4. In this circuit the input amplifier A1 provides input matching, power gain and single to differential conversion for an input frequency f (AC coupled from 50 Ω). The differential distortion amplifier A2 is a standard bipolar linear differential amplifier except that *npn* transistors

Value (Ω)	Number on *starCHIP*™ 1	Tol. ±%	Temp. coeff. ppm/°C	Match ±%
100	144	15	-800	1
200	52	12	-800	.7
1000	46	10	-800	.5
125–500	152	12	-800	.7

Table 1. Thin-film polysilicon resistor data

Device Type	Number on *starCHIP*™ 1	I_C (mA) [peak f_T]	C_{jc} (fF) [$V_{CB}=0$]	R_b (Ω) [peak f_T]
40220	24	2.5	60	45
40420	48	5	100	20
40820	8	10	190	9
41425	12	25	400	4

Table 2. Typical high frequency transistor data

Parameter	Measurement Condition	Min. Value	Typ. Value	Max. Value
h_{FE}	I_C = 2mA, V_{CE} = 4V	40	100	150
V_A	I_C = 2mA, V_{CE} = 4V		25 V	
V_{BE}(ON)	I_C = 5mA, V_{CB} = 0V		.82 V	
BV_{CS}	$I_C = 10\mu$A	30 V	35 V	
BV_{CBO}	$I_C = 10\mu$A	20 V	25 V	
BV_{CEO}	$I_C = 10\mu$A (base open)	12 V	15 V	
BV_{EBO}	$I_E = 10\mu$A	1.5 V	2 V	

Table 3. DC transistor data (currents refer to 40420 device)

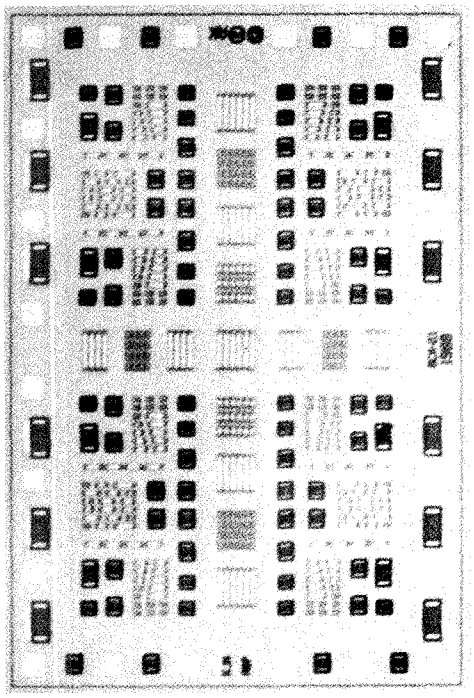

Figure 3. Photograph of the *starCHIP*™ 1 die

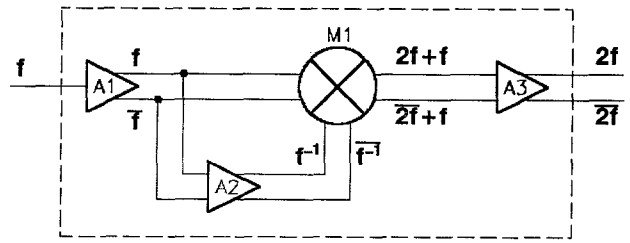

Figure 4. Schematic of frequency doubler

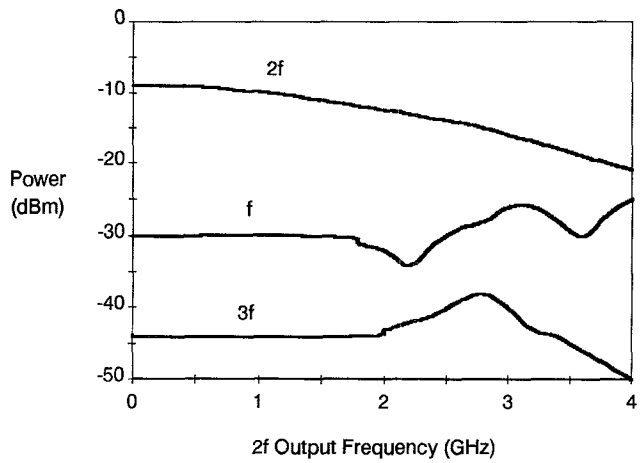

Figure 5. Measured output of frequency doubler versus $2f$ output frequency

with base shorted to collector are used as loads instead of resistors. This non-linear transformation is required since f^{-1} and $\overline{f}^{-1}$ will have an inverse non-linear transformation applied by the LO quad of the Gilbert cell active mixer M1. With the original signal f applied to the RF port, the mixer then has differential outputs $2f$ and $\overline{2f}$ both containing a strong common mode f signal and different DC offsets. The common mode signal is largely removed by an output differential amplifier A3 which also provides output impedance matching. The basic circuit design for this type of wideband doubler is discussed in reference [7] and the actual implementation here is described in detail in reference [8].

This layout uses about 70% of the available devices on *starCHIP*™ 1 and the multiple non-linear transformations test the V_{BE} matching on the array. The measured output power spectrum of either differential channel of a typical frequency doubler is shown in Figure 5. At low output frequencies, typical parts exhibit 1–3 dB $2f$ gain per channel relative to the f input power, > 20 dBc rejection of f, $3f$, $5f$, ... components in the $2f$ outputs and a P_{-1dB} of about -5 dBm. The doublers operated from a single 5 V supply with about 80 mA total current and were tested in a 180 mil glass-metal 8-lead package. As shown in Figure 5, typical parts have a 3 dB bandwidth of about 2 GHz output frequency and $2f > f$ output power to above 4 GHz output frequency.

Wideband Vector Demodulator

Another receiver component successfully implemented on the *starCHIP*™ 1 is a wideband image reject mixer or vector demodulator. A conceptual view of this circuit is given in Figure 6. This design is essentially a mixed analog/digital circuit which utilizes a digital master/slave D flip flop and two matched Gilbert cell active mixers. The flip flop is connected as an asynchronous toggle which divides an input 2LO frequency into 0° and 90° phase LO signals. These LO signals are then used to drive the in phase (I) and quadrature phase (Q) Gilbert cell active mixers. Since a single-ended 2LO input is required for the demodulator, swept frequency testing used the previously-described frequency doubler to provide the 2LO input. Both the 2LO and RF inputs provide port-insensitive impedance matching to 50 Ω and single to differential conversions. Differential output buffers with VSWR< 2 are provided for the quadrature IF outputs. The design of this circuit is discussed in detail in reference [8].

Measured conversion gain of a typical IF port is given in Figure 7 for a fixed IF=70 MHz, LO=−10 dBm (input to the frequency doubler). A time domain view of the I

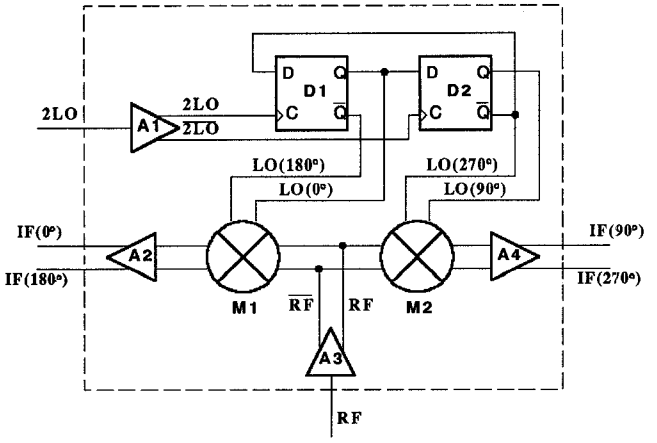

Figure 6. Schematic of vector demodulator

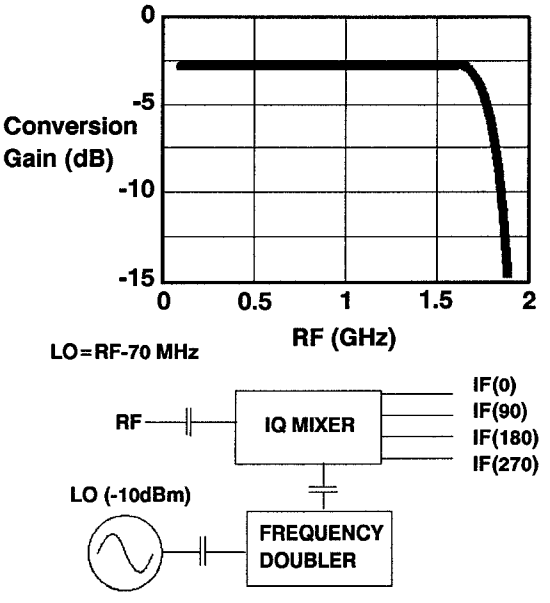

Figure 7. Conversion gain of vector demodulator and frequency doubler combination versus RF frequency

and Q (0° and 90° IF) outputs is given in Figure 8. In Figure 9, a vector analyzer is employed to plot Q versus I and thus illustrate the excellent 90° phase and magnitude match between ports. Typical parts have quadrature errors of less than 5 ° and gain mismatches of less than .5 dB which can provide for image rejections of greater than 25 dB. The demodulator operates from a single 5 V supply and draws about 80 mA.

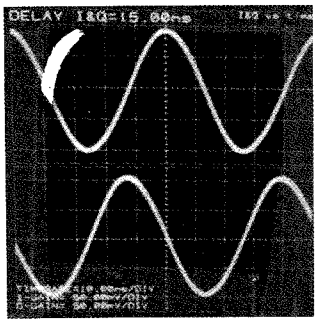

Figure 8. Time domain output of I and Q channels of vector demodulator

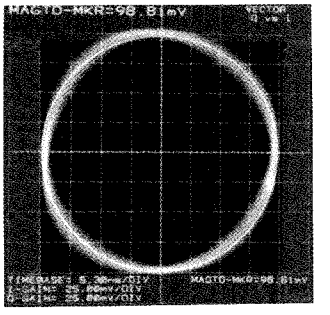

Figure 9. Plot of Q channel versus I channel of vector demodulator

Wideband Limiting Amplifiers

Several other monolithic receiver components have also been prototyped on the *starCHIP*™ – 1 analog transistor array. Wideband limiting amplifiers employing one or two stages have been fabricated. The designs use a balanced amplifier version of the circuit originally proposed in [9]. The limiting amplifiers produce approximately 15 or 40 dB of gain respectively with bandwidths to about 2 GHz.

Wideband Phase Detector with On-Chip VCO

Active phase detectors with on-chip VCO components have also been implemented on the *starCHIP*™ – 1 array for use in phase-locked loops. The phase detectors have a DC output swing of 1000 mV, feature a 4 GHz bandwidth, and require an input of only −20 dBm. The VCO is realized with a wideband on-chip negative resistance cell coupled to a simple off-chip tank circuit.

Conclusions

The *starCHIP*™ 1 analog transistor array is an effective prototype vehicle for RF/microwave components. The *starCHIP*™ 1 provides an uncommitted array of microwave silicon bipolar transistors and thin-film resistors which can easily be connected to perform a desired function. The total design cycle time is greatly reduced by this semi-custom approach and the lower non-recurring costs compared with full-custom ICs makes the *starCHIP*™ 1 economically attractive for low volume applications.

Acknowledgements

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